



Introduction to Digital Design Using Digilent FPGA Boards - VHDL Edition

Richard E. Haskell and Darrin M. Hanna

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This book uses 30 examples to show you how to get started designing digital circuits in VHDL and using block diagrams, simulate them, and quickly and easily download them to your Basys™ or Nexys2™ board. Get up and running quickly - step-by-step, by example! A major revolution in digital design has taken place over the past decade. Field programmable gate arrays (FPGAs) can now contain over a million equivalent logic gates and tens of thousands of flip-flops. This means that it is not possible to use traditional methods of logic design involving the drawing of logic diagrams when the digital circuit may contain thousands of gates. The reality is that today digital systems are designed by writing software in the form of hardware description languages (HDLs). The most common HDLs used today are VHDL and Verilog. Both are in widespread use. When using these hardware description languages the designer typically describes the behavior of the logic circuit rather than writing traditional Boolean logic equations. Computer-aided design tools are used to both simulate the VHDL or Verilog design and to synthesize the design to actual hardware. This book assumes no previous knowledge of digital design. We will use Active-HDL from Aldec to design, simulate, synthesize, and implement our digital designs. A free student edition of Active-HDL simulator is available from Aldec Inc (www.aldec.com). To synthesize your design to a Spartan3E FPGA, you will need to download the Free ISE WebPACK from Xilinx Inc. (www.xilinx.com). The Xilinx synthesis tools are called from within the Aldec Active-HDL integrated GUI. We will use the ExPort utility to download your synthesized design to the Spartan3E FPGA. ExPort is part of the Adept software suite that you can download free from Digilent, Inc.

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